

# HEF4043B

## Quad R/S latch with 3-state outputs

Rev. 06 — 11 November 2008

Product data sheet

## 1. General description

The HEF4043B is a quad R/S latch with 3-state outputs with a common output enable input (OE). Each latch has an active HIGH set input (1S to 4S), an active HIGH reset input (1R to 4R) and an active HIGH 3-state output (1Q to 4Q).

When OE is HIGH, the latch output (nQ) is determined by the nR and nS inputs as shown in [Table 3](#). When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. The high impedance off-state feature allows common bussing of the outputs.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input. It is also suitable for use over the industrial ( $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ) temperature range.

## 2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

## 3. Applications

- Four-bit storage with output enable

## 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package		Version
	Name	Description	
HEF4043BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF4043BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

**5. Functional diagram**

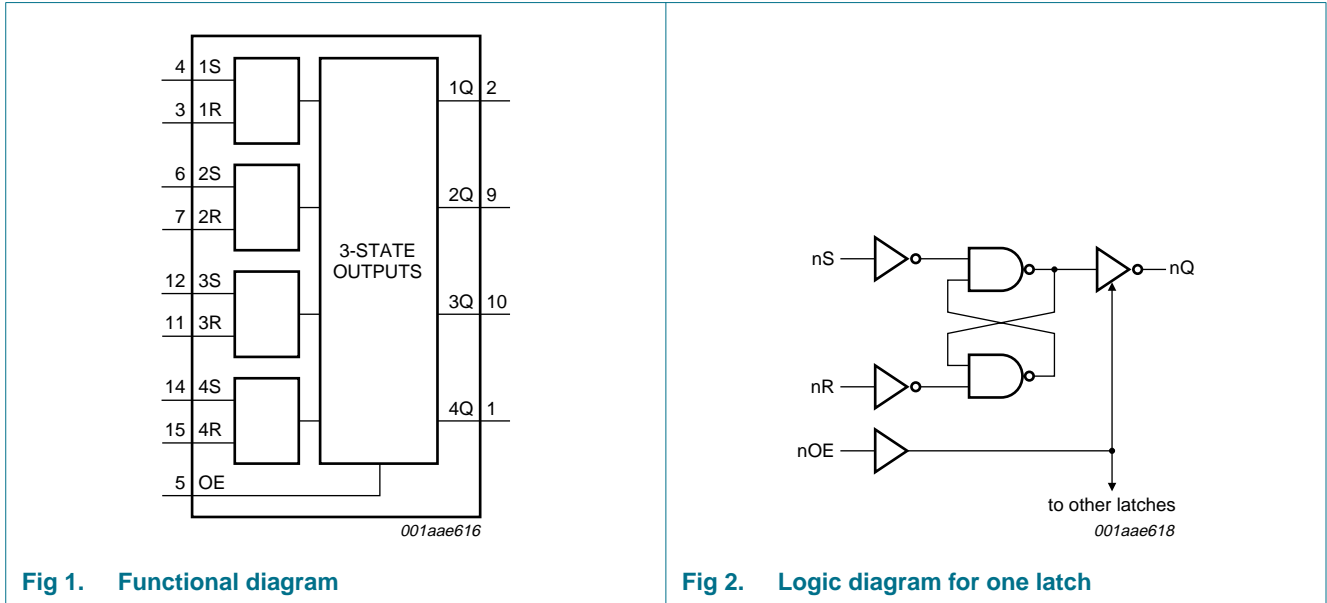


Fig 1. Functional diagram

Fig 2. Logic diagram for one latch

**6. Pinning information**

**6.1 Pinning**

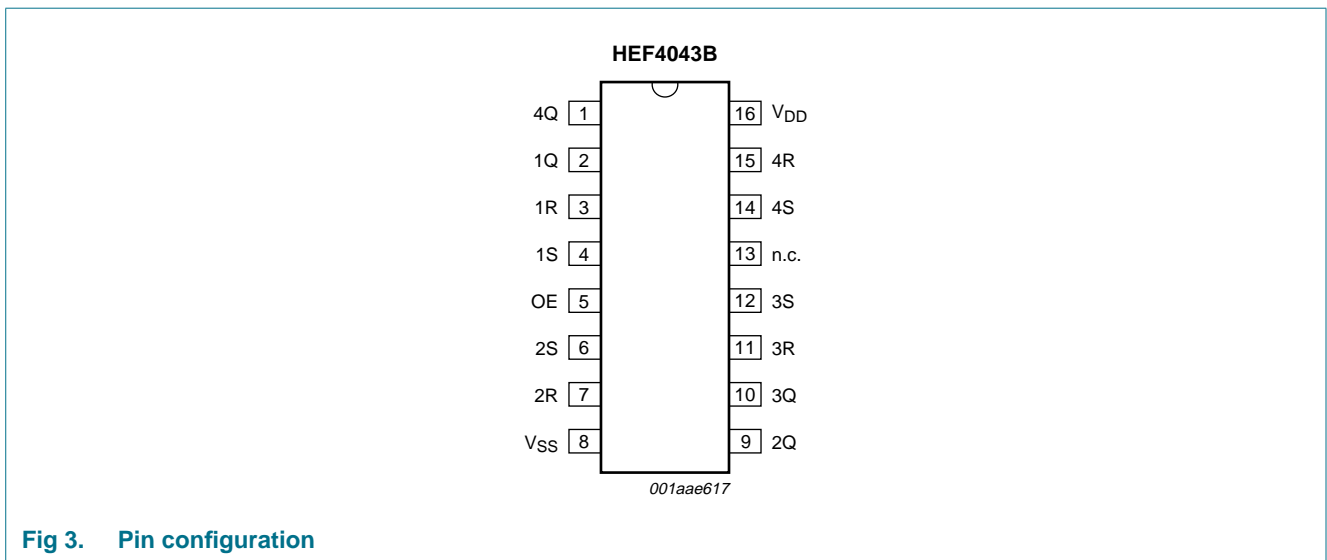


Fig 3. Pin configuration

## 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q to 4Q	2, 9, 10, 1	3-state buffered latch output
1R to 4R	3, 7, 11, 15	reset input (active HIGH)
1S to 4S	4, 6, 12, 14	set input (active HIGH)
OE	5	common output enable input
V <sub>SS</sub>	8	ground supply voltage
n.c.	13	not connected
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs			Output
OE	nS	nR	nQ
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance state.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DD</sub>	supply voltage		-0.5	+18	V	
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
I <sub>I/O</sub>	input/output current		-	±10	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
T <sub>amb</sub>	ambient temperature		-40	+85	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> -40 °C to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output	-	100	mW	

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage		3	-	15	V
V <sub>I</sub>	input voltage		0	-	V <sub>DD</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>DD</sub> = 5 V	-	-	3.75	ns/V
		V <sub>DD</sub> = 10 V	-	-	0.5	ns/V
		V <sub>DD</sub> = 15 V	-	-	0.08	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

V<sub>SS</sub> = 0 V; V<sub>I</sub> = V<sub>SS</sub> or V<sub>DD</sub> unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub>   < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-1.7	-	-1.4	-	-1.1	-	mA
		V <sub>O</sub> = 4.6 V	5 V	-0.52	-	-0.44	-	-0.36	-	mA
		V <sub>O</sub> = 9.5 V	10 V	-1.3	-	-1.1	-	-0.9	-	mA
		V <sub>O</sub> = 13.5 V	15 V	-3.6	-	-3.0	-	-2.4	-	mA
I <sub>OL</sub>	LOW-level output current	V <sub>O</sub> = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V <sub>O</sub> = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I <sub>I</sub>	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	nQ output HIGH; returned to V <sub>DD</sub>	15 V	-	1.6	-	1.6	-	12.0	μA
		nQ output LOW; returned to V <sub>SS</sub>	15 V	-	1.6	-	1.6	-	12.0	μA

**Table 6. Static characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = 25\text{ }^{\circ}\text{C}$		$T_{amb} = 85\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance			-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; For waveforms and test circuit see [Section 12](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	nR $\rightarrow$ nQ; see <a href="#">Figure 4</a>	5 V	[1] $63\text{ ns} + (0.55\text{ ns/pF})C_L$	-	90	180	ns
			10 V	$24\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
$t_{PLH}$	LOW to HIGH propagation delay	nS $\rightarrow$ nQ; see <a href="#">Figure 4</a>	5 V	[1] $38\text{ ns} + (0.55\text{ ns/pF})C_L$	-	65	135	ns
			10 V	$14\text{ ns} + (0.23\text{ ns/pF})C_L$	-	25	50	ns
			15 V	$7\text{ ns} + (0.16\text{ ns/pF})C_L$	-	15	35	ns
$t_t$	transition time	nQ output; see <a href="#">Figure 4</a>	5 V	[1] [2] $10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	OE $\rightarrow$ nQ; see <a href="#">Figure 5</a>	5 V		-	45	90	ns
			10 V		-	20	35	ns
			15 V		-	10	25	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	OE $\rightarrow$ nQ; see <a href="#">Figure 5</a>	5 V		-	50	100	ns
			10 V		-	20	40	ns
			15 V		-	10	25	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	OE $\rightarrow$ nQ; see <a href="#">Figure 5</a>	5 V		-	25	50	ns
			10 V		-	15	30	ns
			15 V		-	10	25	ns
$t_{PZL}$	OFF-state to LOW propagation delay	OE $\rightarrow$ nQ; see <a href="#">Figure 5</a>	5 V		-	40	80	ns
			10 V		-	20	45	ns
			15 V		-	15	35	ns
$t_W$	pulse width	nS input HIGH; minimum width; see <a href="#">Figure 4</a>	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns
		nR input HIGH; minimum width; see <a href="#">Figure 4</a>	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

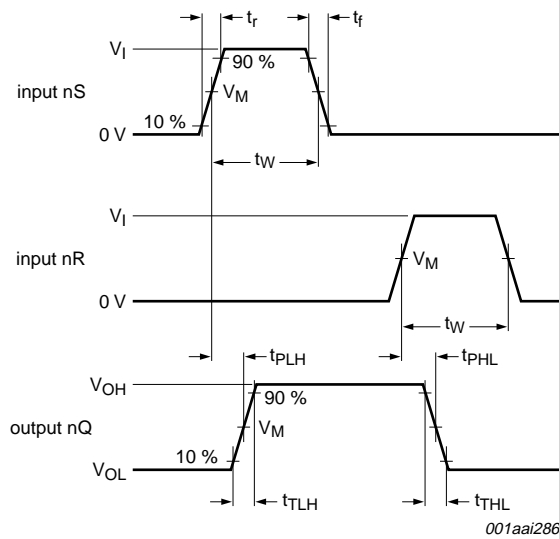
[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz;
		10 V	$P_D = 4400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz;
		15 V	$P_D = 11400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF;
				$V_{DD}$ = supply voltage in V;
				$\Sigma(C_L \times f_o)$ = sum of the outputs.

## 12. Waveforms



$t_r$  and  $t_f$  are the input rise and fall times

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Transition times: transition time ( $t_t$ ) = HIGH LOW ( $t_{THL}$ ) or LOW HIGH ( $t_{TLH}$ ) transition times.

Measurement points are given in [Table 9](#) and test data is given in [Table 10](#).

**Fig 4. Input minimum set (nS) and reset (nR) pulse widths, inputs nS or nR to latch output (nQ) propagation delay and nQ transition time**

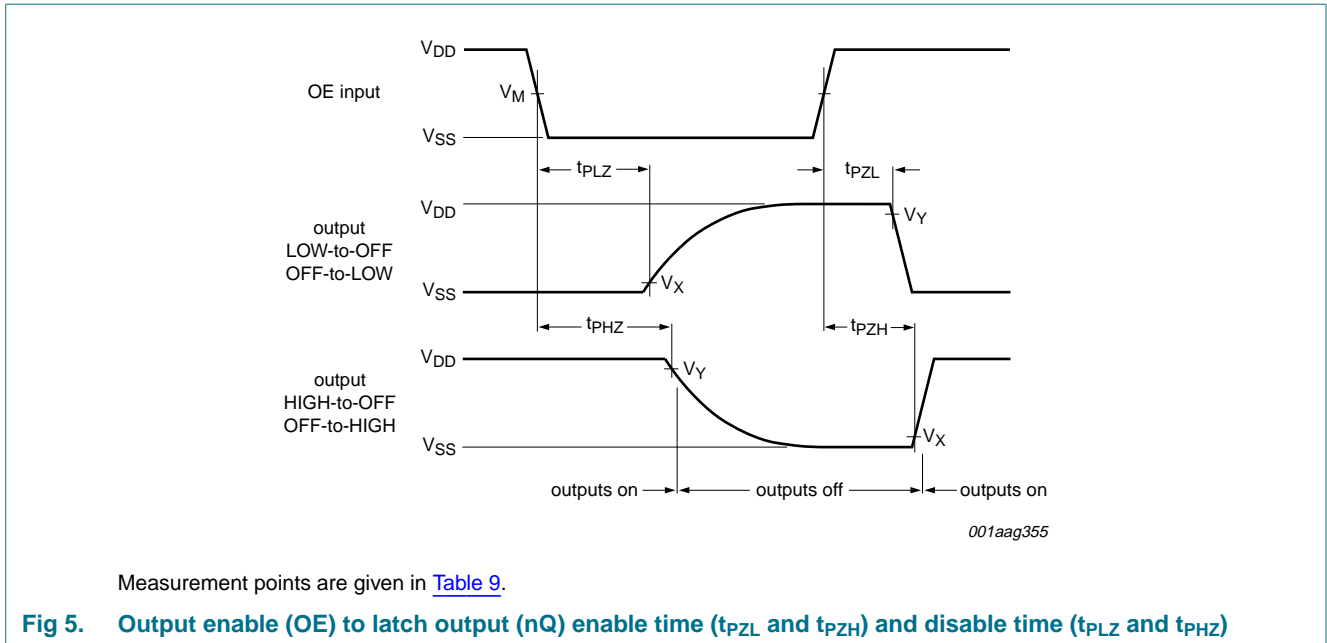
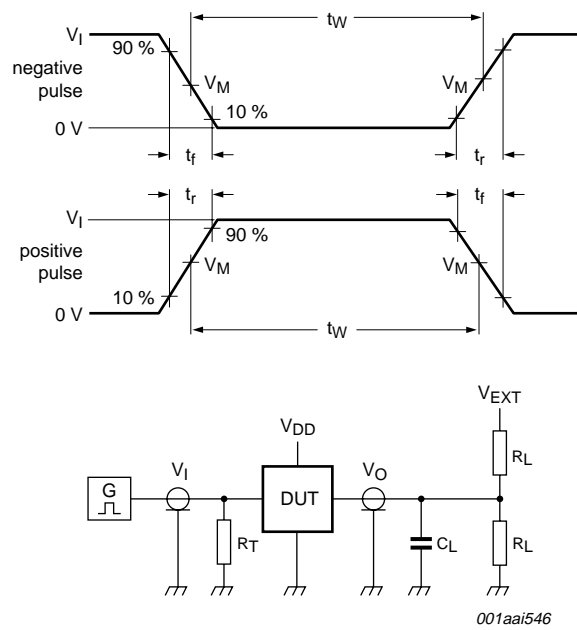


Table 9. Measurement points

Supply voltage	Input		Output		
$V_{DD}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
5 V to 15 V	$V_{DD}$ or 0 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



Test and measurement data is given in [Table 10](#).

Definitions test circuit:

DUT = Device Under Test.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

**Fig 6. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
5 V to 15 V	$V_{DD}$	$\leq 20$ ns	50 pF	1 k $\Omega$	open	$2V_{DD}$	GND



13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

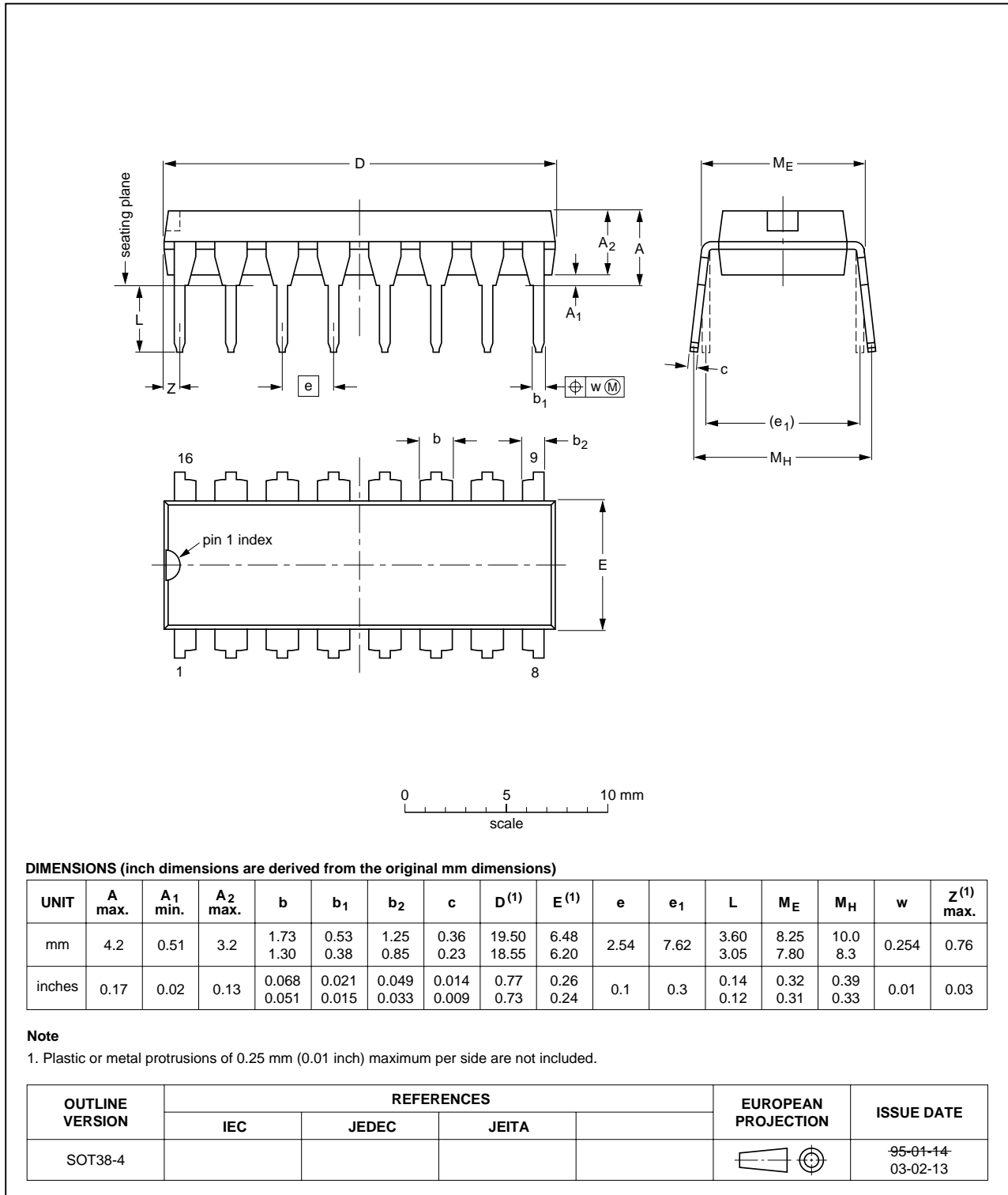


Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

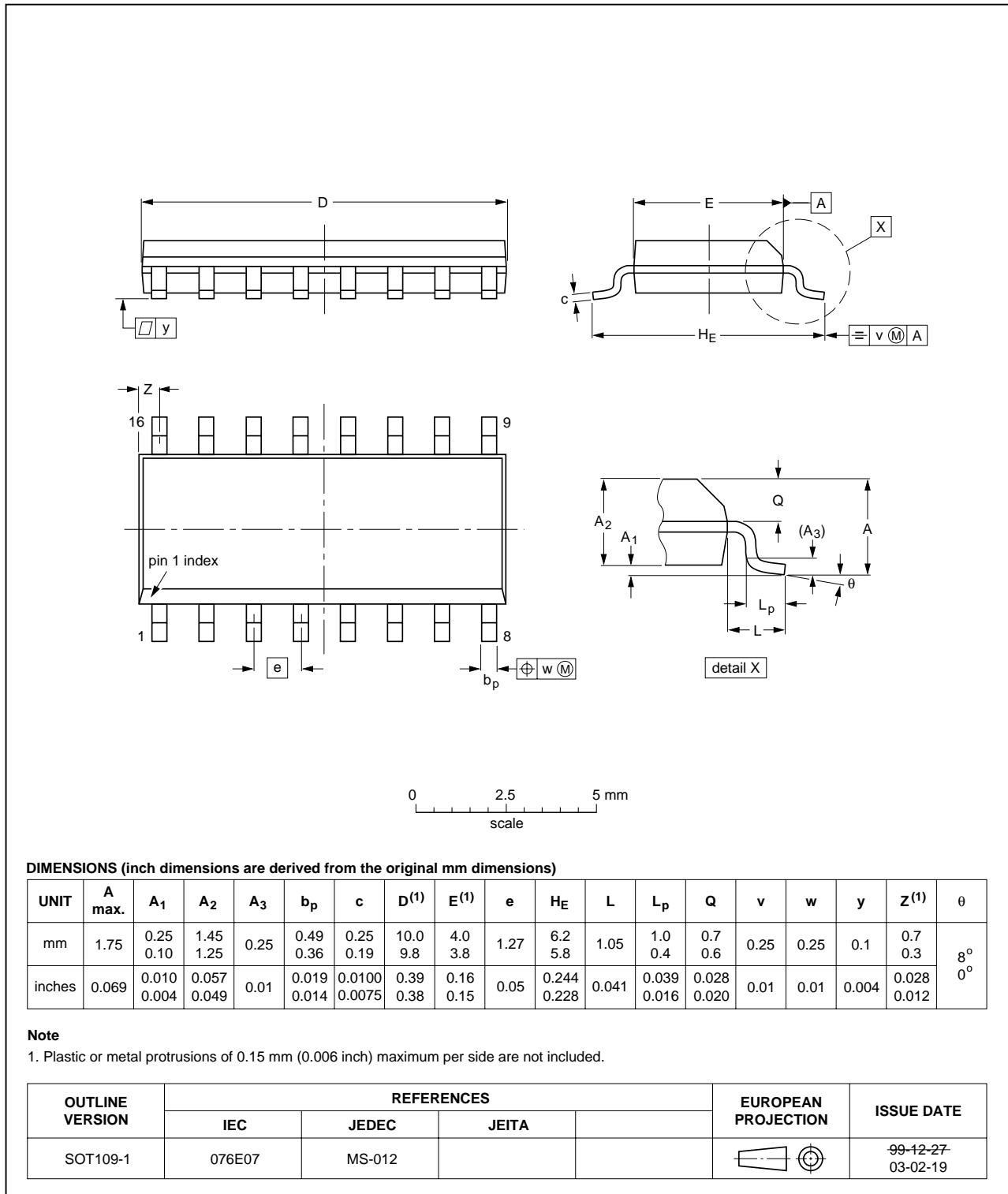


Fig 8. Package outline SOT109-1 (SO16)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4043B_6	20081111	Product data sheet	-	HEF4043B_5
Modifications:	<ul style="list-style-type: none"> <li>• Maximum <math>T_{amb}</math> changed to 85 °C and <math>T_{amb} = 125</math> °C parameter data removed throughout.</li> <li>• <a href="#">Section 1 “General description”</a> temperature range statement modified.</li> <li>• <a href="#">Table 6 “Static characteristics”</a> <math>I_{OH}</math>, <math>I_{OL}</math>, <math>I_{OZ}</math> and <math>I_{DD}</math> values updated.</li> </ul>			
HEF4043B_5	20080729	Product data sheet	-	HEF4043B_4
HEF4043B_4	20080710	Product data sheet	-	HEF4043B_CNV_3
HEF4043B_CNV_3	19950101	Product specification	-	HEF4043B_CNV_2
HEF4043B_CNV_2	19950101	Product specification	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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